

GA-880GM-D2H

Revision : 4.0

PAGE	TITLE	9M880GD2H-00
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU HYPER TRANSPORT	
05	CPU DDRIII MEMORY	
06	CPU CONTROL	
07	CPU POWER & GND	
08	DDRIII CHANNEL A, B	
09	RS780 HT-LINK I/F	
10	RS780 SYSTEM I/F,STRAP	
11	RS780 POWER & GND	
12	RTM880T-792-VB-GRT	
13	ATI SB710 PCIE/PCI/CPU/LPC	
14	ATI SB710 ACPI/USB/GPIO/AUDIO	
15	ATI SB710 SATA/SPI/IDE/HWM	
16	ATI SB710 POWER & GND	
17	PCI EXPRESS x16 ,x1	
18	PCI SLOT	
19	LAN AR8151/8152	
20	AUDIO ALC887-VD2 AUDIO JACK	
21	RGB, COM, F_USB	
22	IT8720 LPC IO ,Dual-BIOS, KB/MS	
23	FAN/HWMO ,USB	
24	ATX, FRONT PANEL	
25	VCORE (PWMISL6324+6609)	

PAGE	TITLE
26	POWER SEQUENCE
27	NB/SB POWER, VCC12HT, VDDA25 ,VCC12_Dual
28	DDRIII POWER, VCC18
29	HDMI , DVI



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Title COVER SHEET		
Size Custom	Document Number GA-880GM-D2H	Rev 4.0
Date: Thursday, August 25, 2011	Sheet 1	of 29

Model Name:GA-880GM-D2H

Component value change history

Version: 4.0

P-Code:

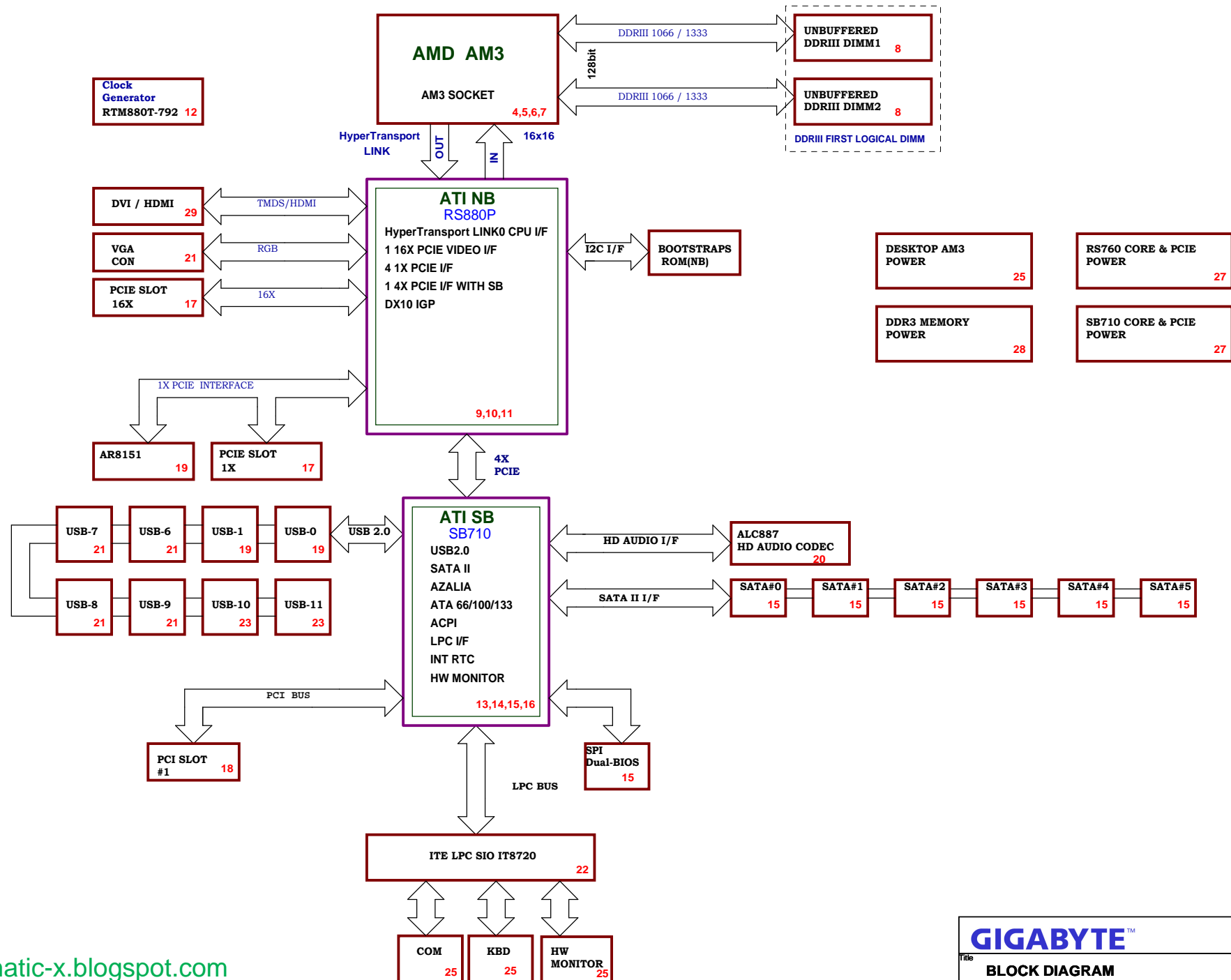
[illegible]

Circuit or PCB layout change for next version

[illegible]

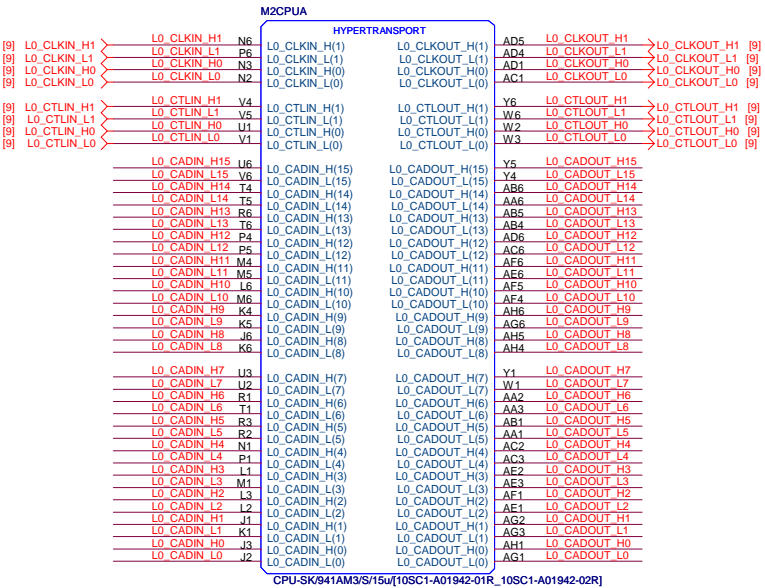
GIGABYTE™			
Title BOM & PCB HISTORY			
Size	Document Number		Rev
Custom	GA-880GM-D2H		4.0
Date:	Thursday, August 25, 2011	Sheet	2 of 29

RS880P CUSTOMER DESKTOP DESIGN



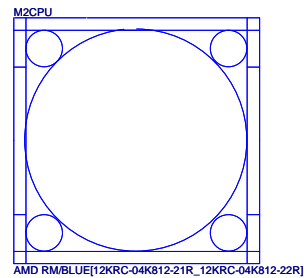
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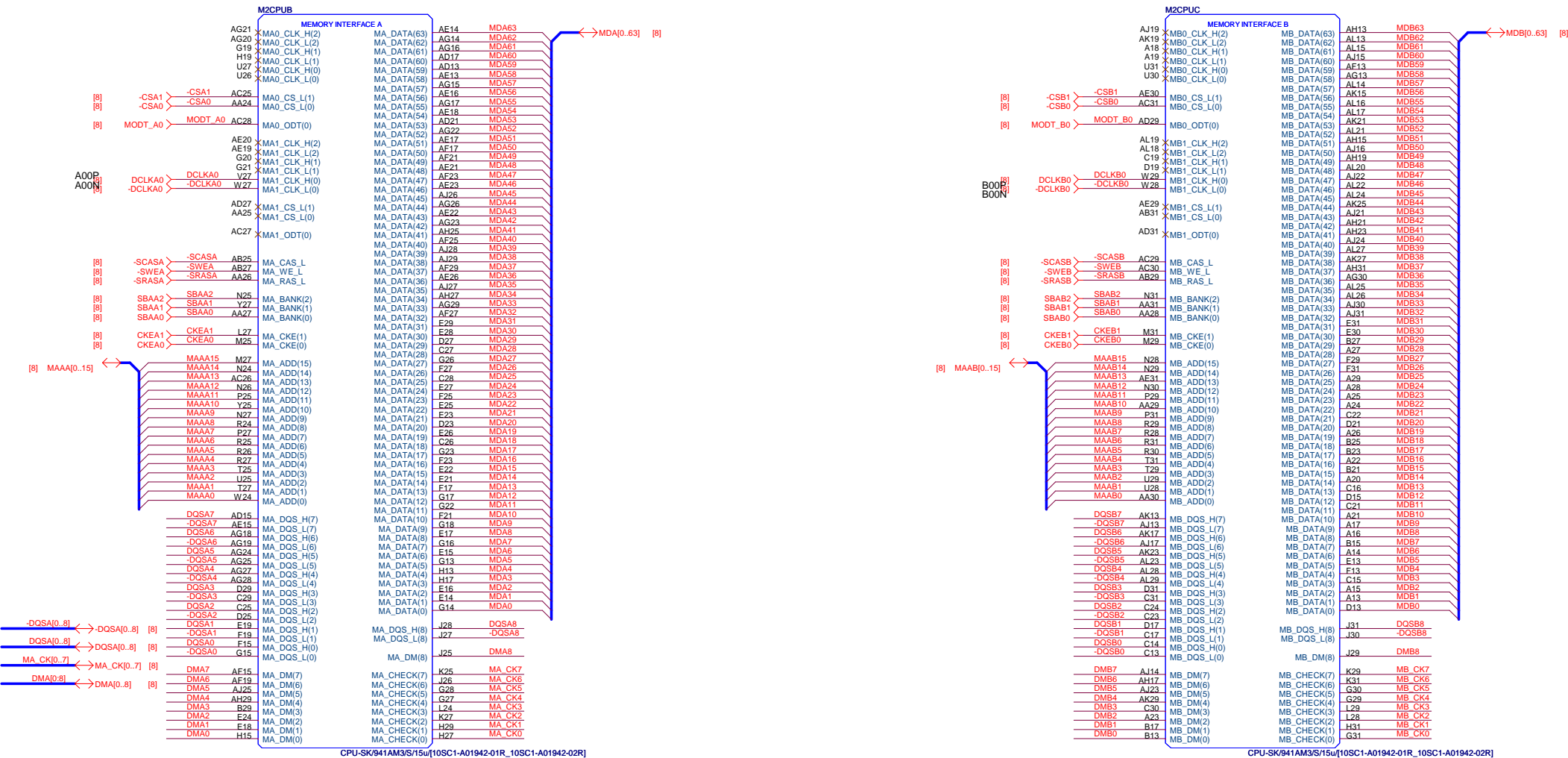
L0_CADOUT_L[0..15] [9]
L0_CADOUT_H[0..15] [9]



CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

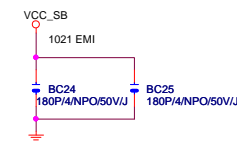
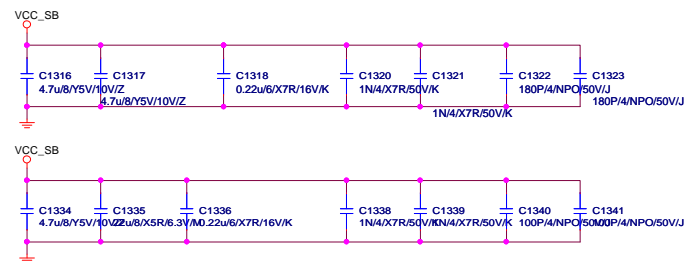
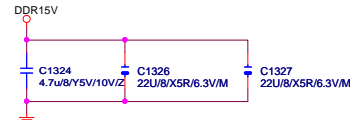
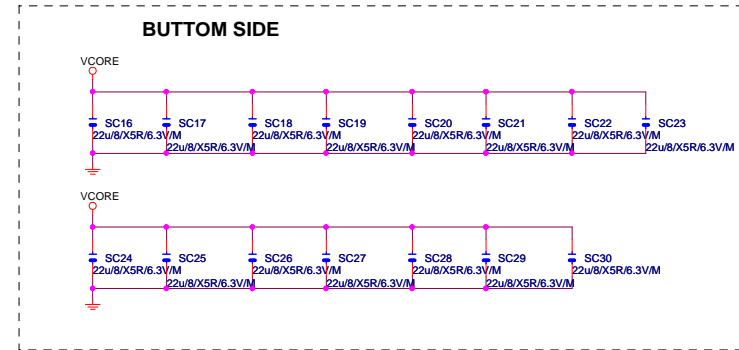
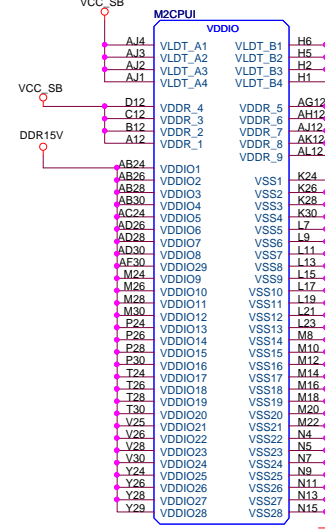
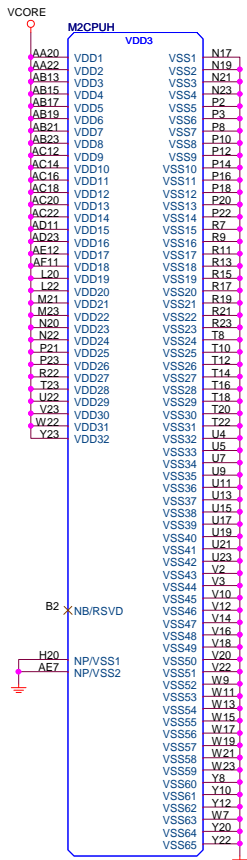


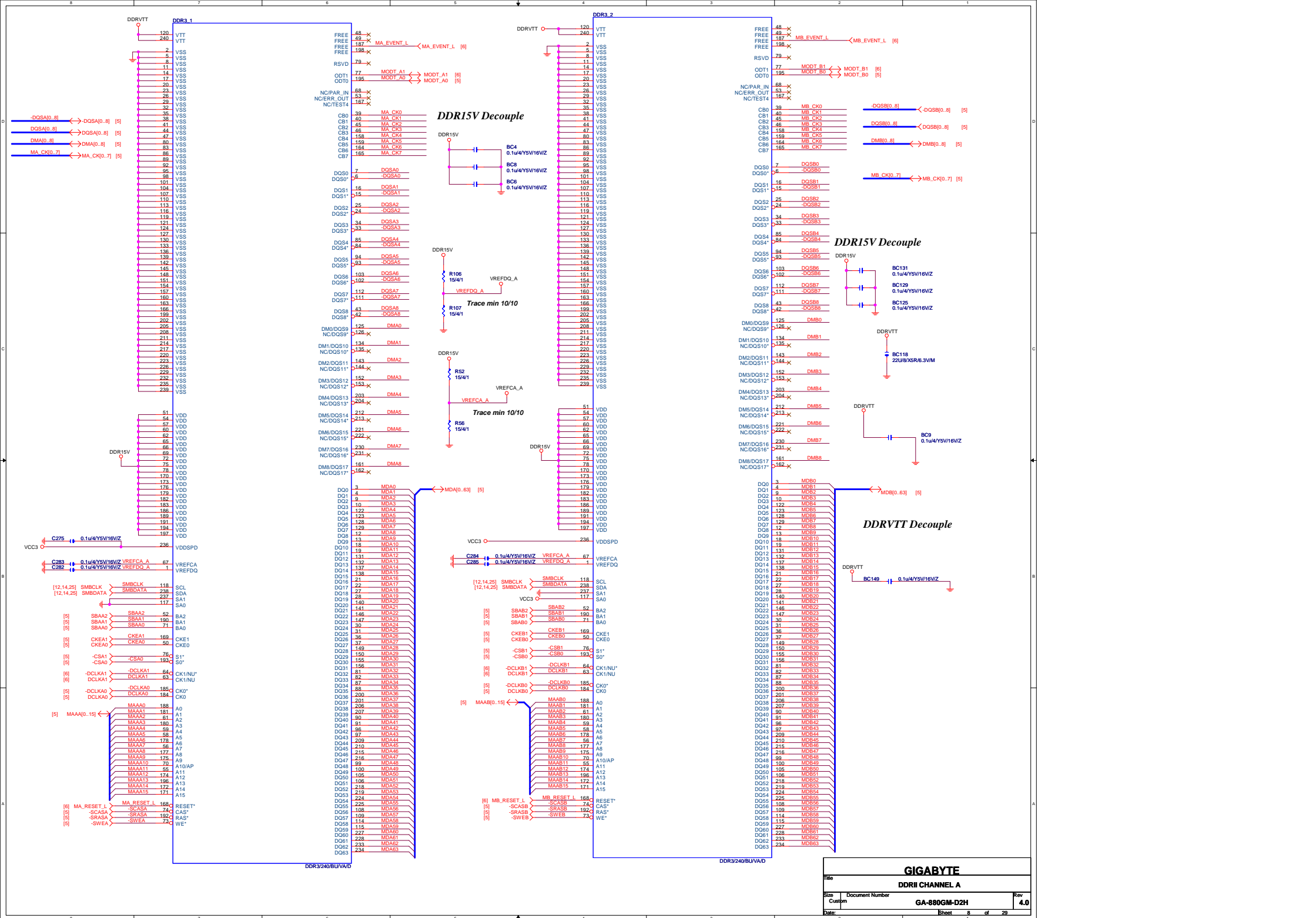


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CPU DDRII MEMORY

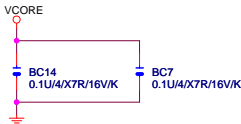
Size	Document Number	Rev
Custom	GA-880GM-D2H	4.0
Date:	Thursday, August 25, 2011	Sheet 5 of 29





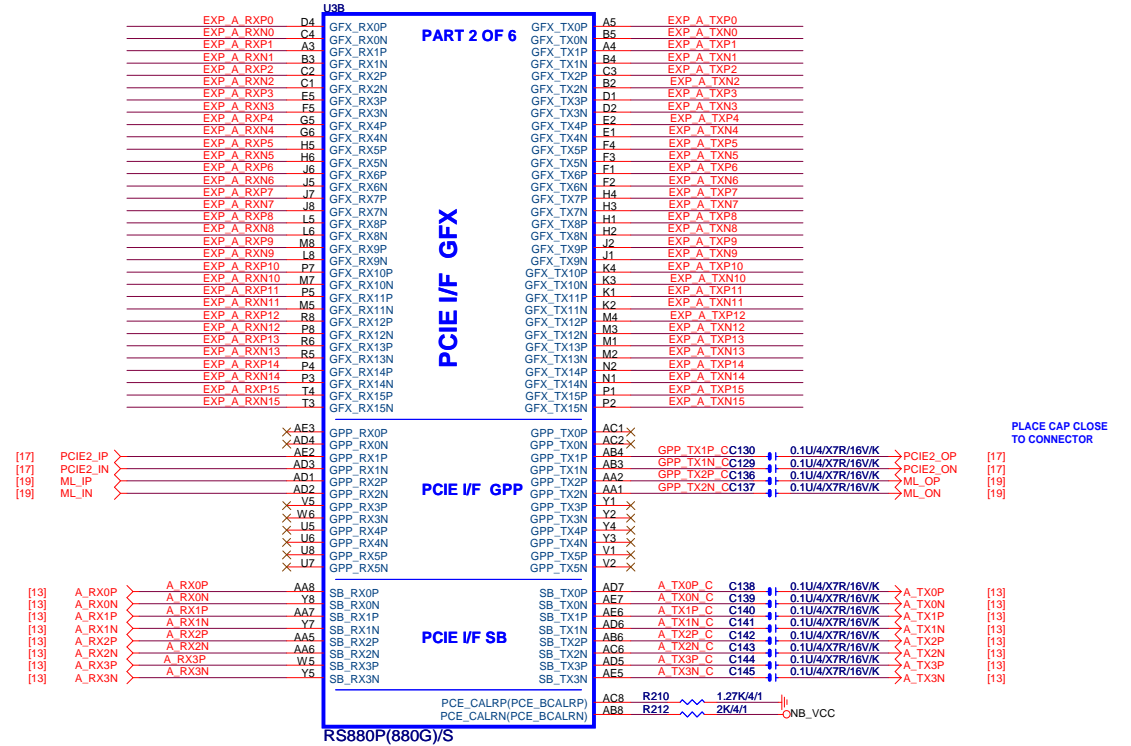
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L0_CADIN_H[0..15] <L0_CADIN_H[0..15] [4]

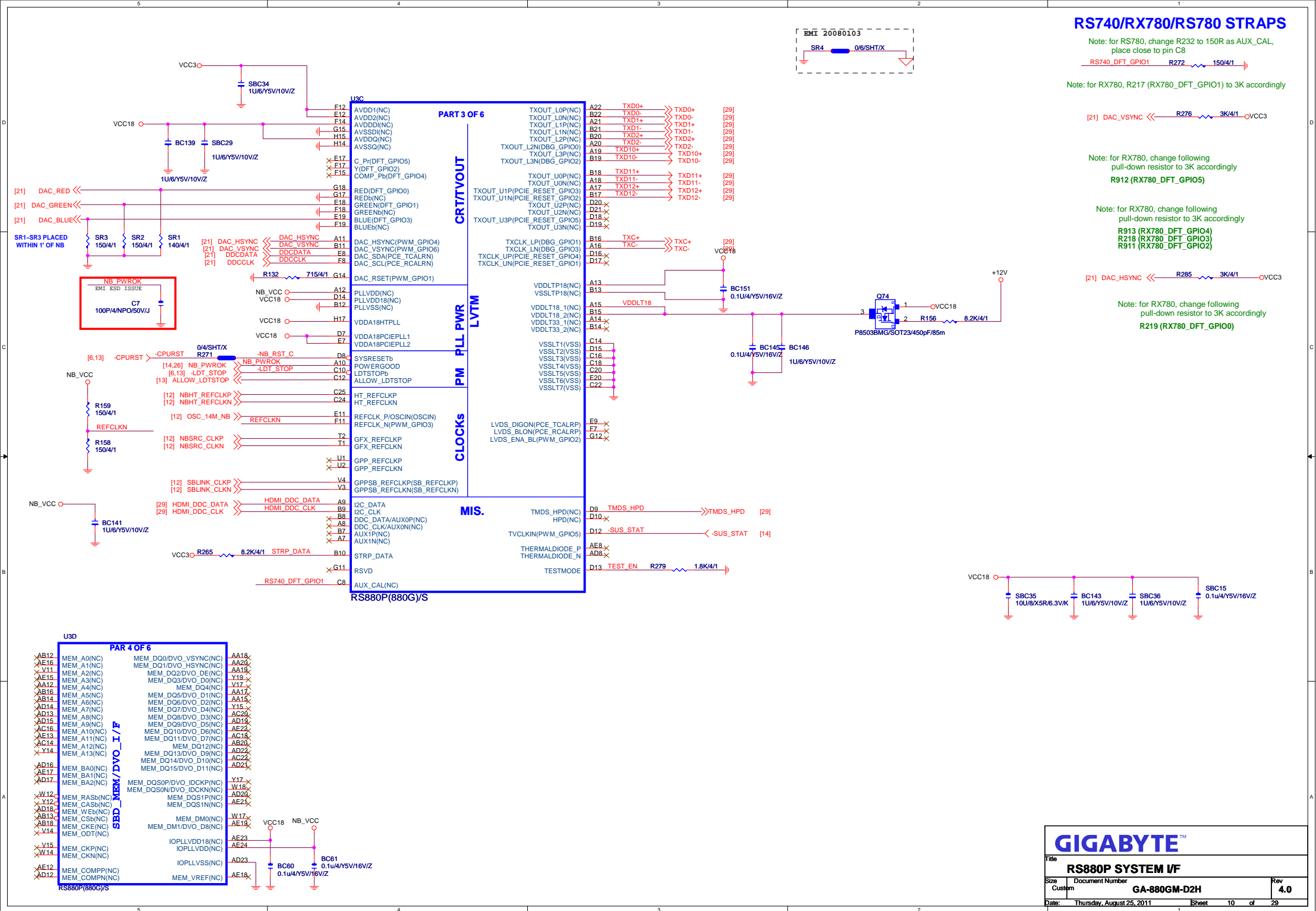
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L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] [4]

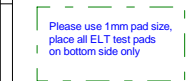


EXP_A_RXP[0..15] >>>EXP_A_RXP[0..15] [17]
EXP_A_RXN[0..15] >>>EXP_A_RXN[0..15] [17]

EXP_A_TXP[0..15] >>>EXP_A_TXP[0..15] [17]
EXP_A_TXN[0..15] >>>EXP_A_TXN[0..15] [17]

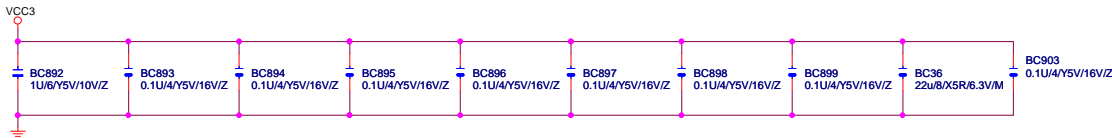




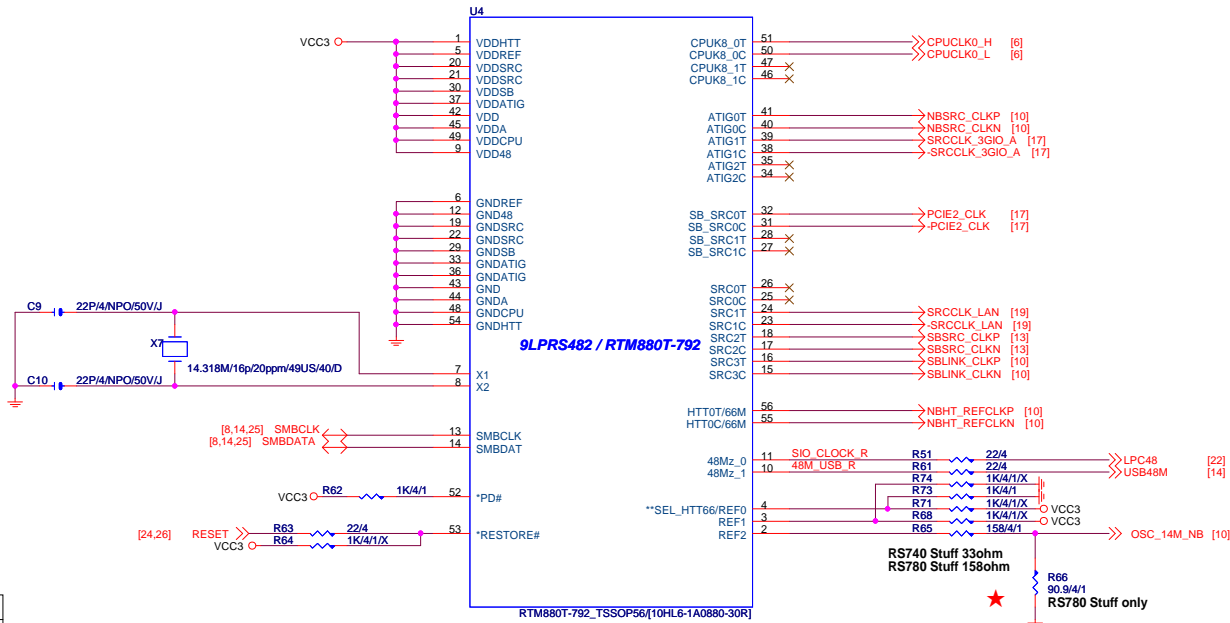


PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC



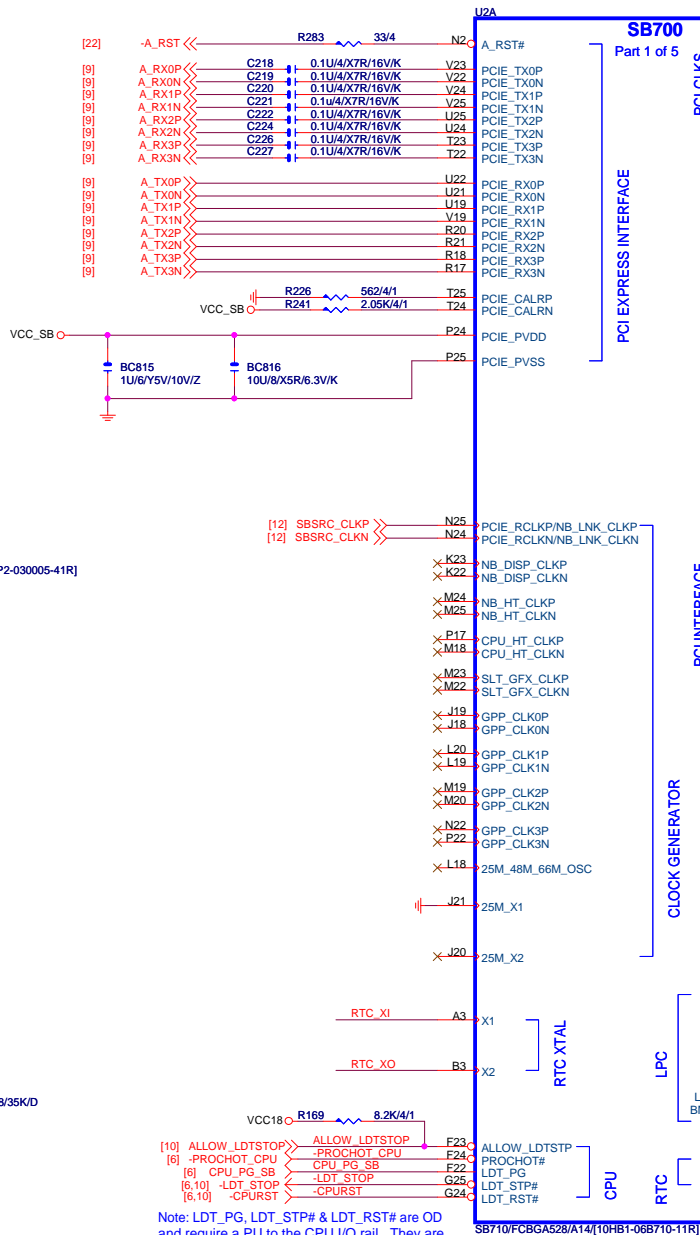
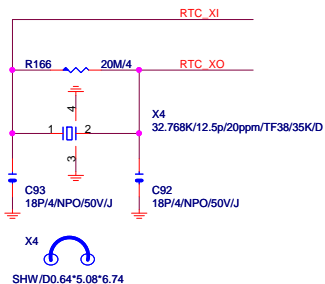


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN





SB_HS/[12SP2-030005-42R_12SP2-030005-43R_12SP2-030005-41R]



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



PCI EXPRESS INTERFACE

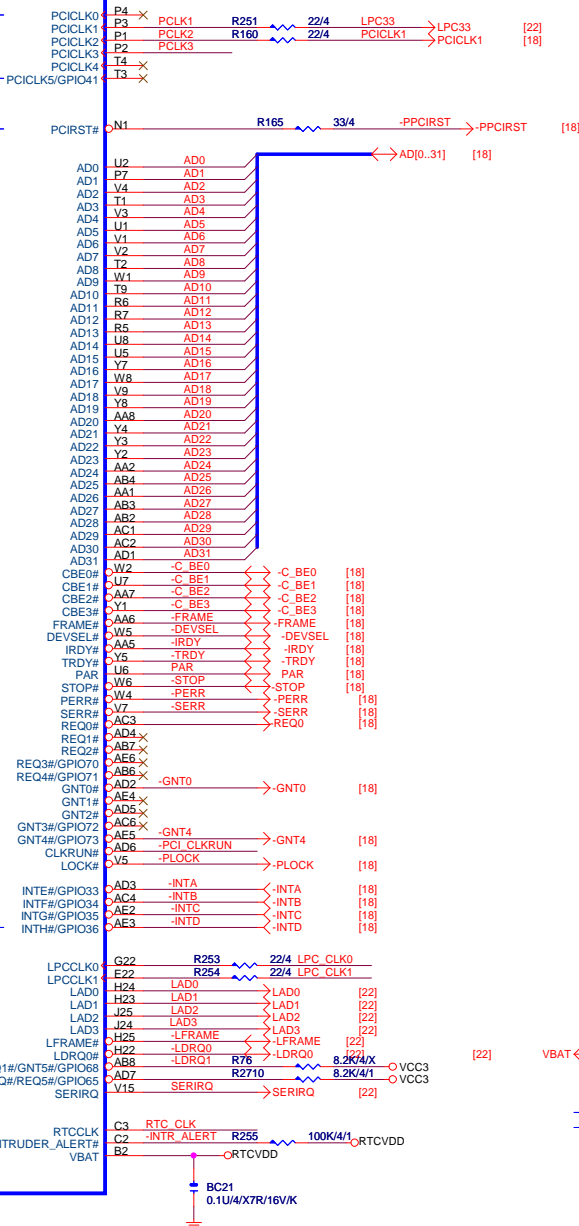
PCI INTERFACE

CLOCK GENERATOR

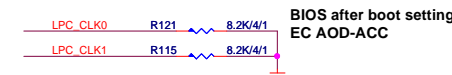
LPC

27

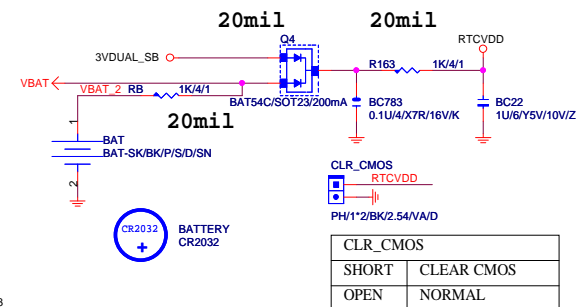
710-1



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT



	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED	CLKGEN DISABLED
	DEFAULT	DEFAULT

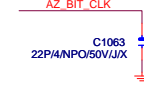
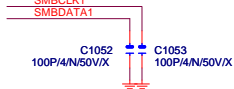
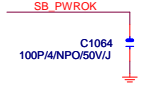
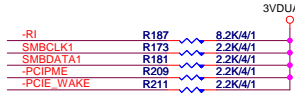
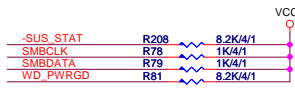


NOT ADD ICT FOR RTCVDD PIN

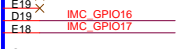
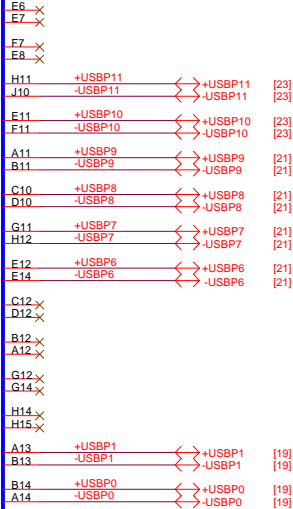
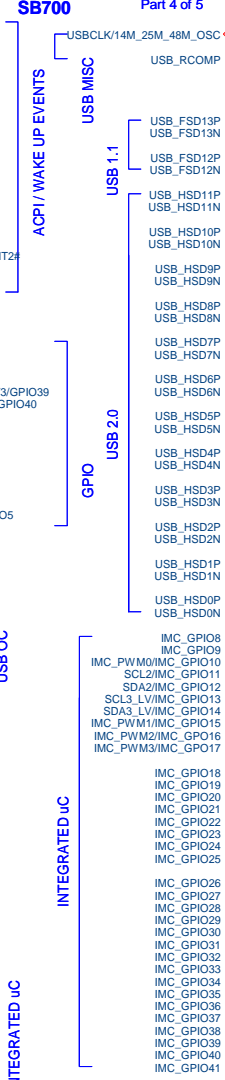
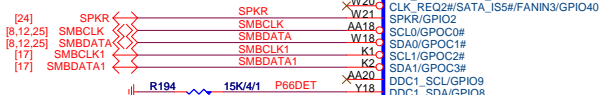
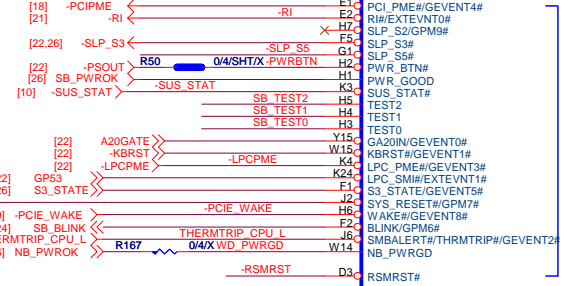
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Title	ATI SB710 PCIE/PC/CPU/LPC
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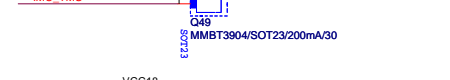
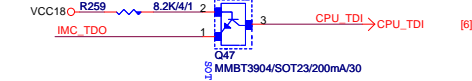
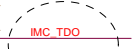
Size	Document Number	Rev
Custom	GA-880GM-D2H	4.0
Date:	Thursday, August 25, 2011	Sheet 13 of 29



AZ_RST#
PULL HIGH ENABLE PCI
PULL LOW DISABLE PCI
MEM BOOT
MEM BOOT
DEFAULT



AOD Extreme



USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO17 IMC_GPIO16

ROM TYPE:

H, H = Reserved

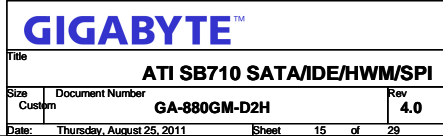
H, L = SPI ROM DEFAULT

L, H = LPC ROM

L, L = FWH ROM

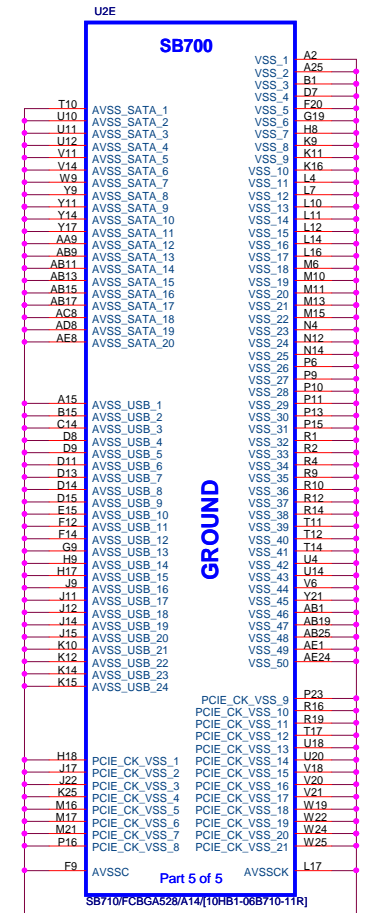
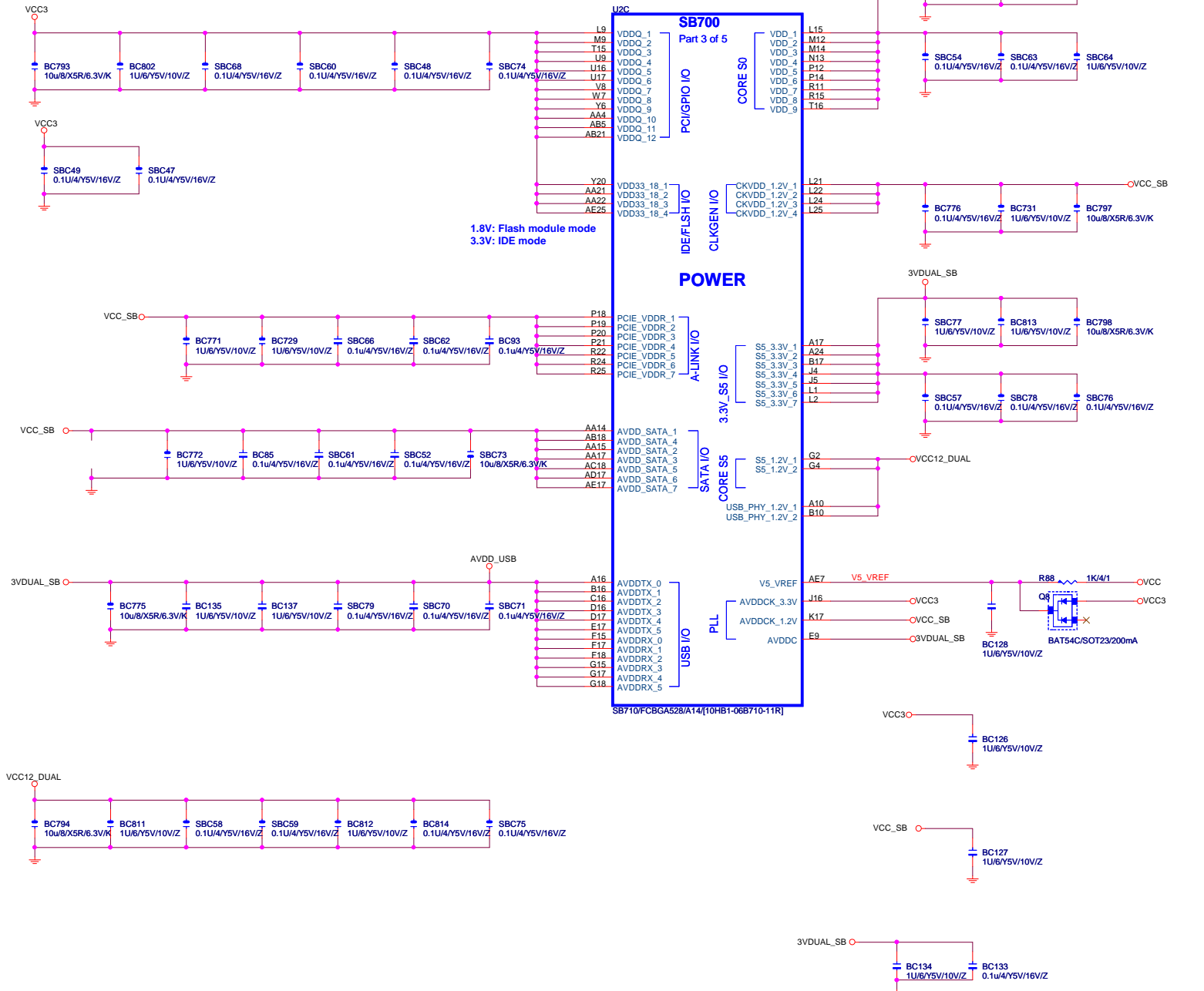
GIGABYTE

Title ATI SB710 ACPI/USB/GPIO/AUDIO		
Size Custom	Document Number GA-880GM-D2H	Rev 4.0
Date: Thursday, August 25, 2011 Sheet 14 of 29		

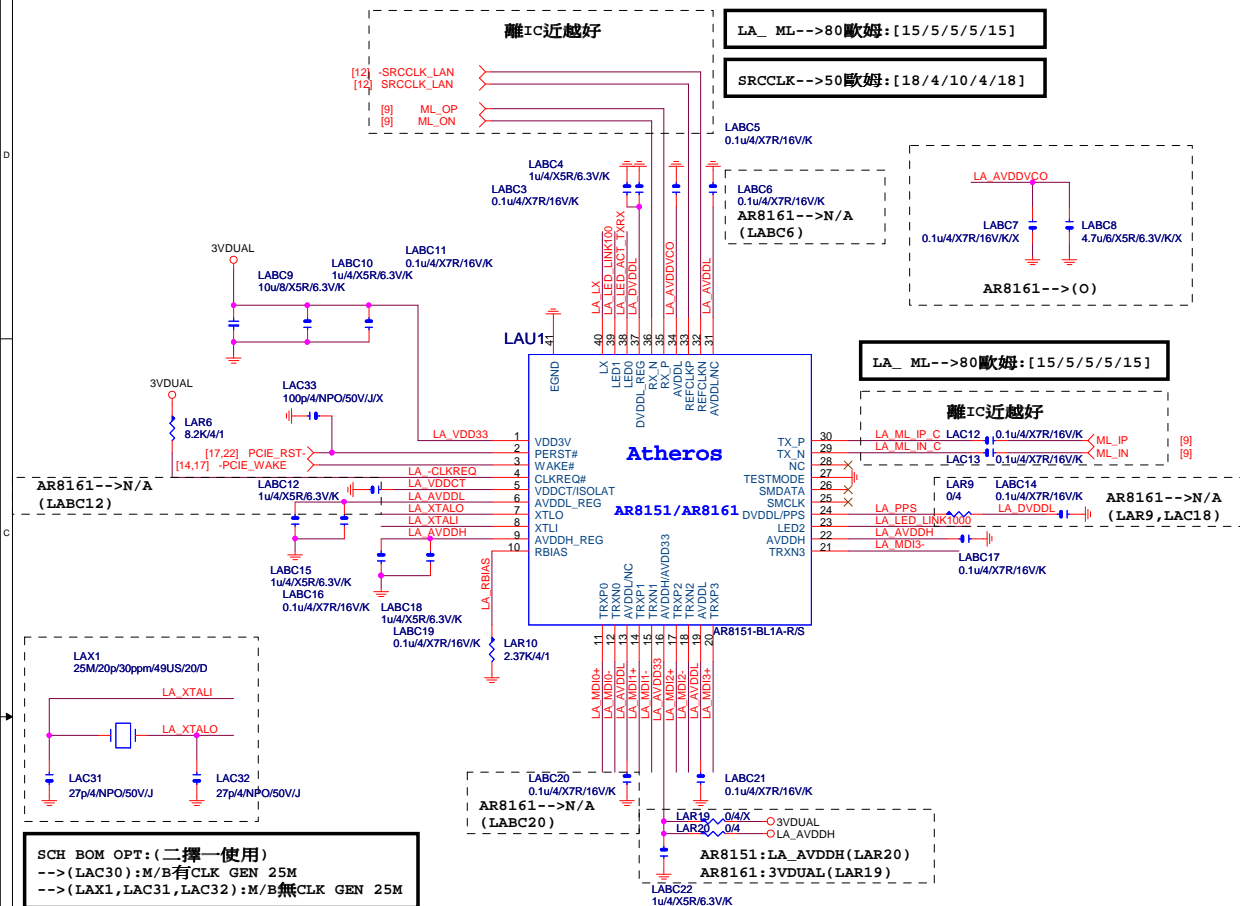




PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



LAN:AR8151/AR8161

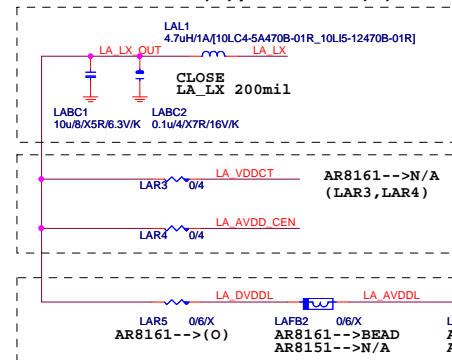


LAN POWER

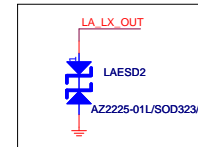
NEW DESIGN ONLY FOR INTERNAL SWR

AR8151:LAR3(O),LAR5(X)

AR8161: LAR5(O), LAR3/LAR4(X)



EMI Request
Put on LAR4



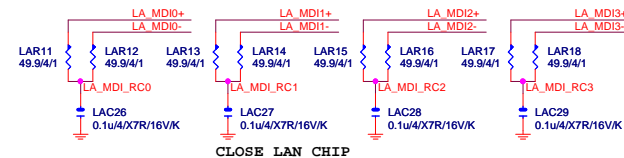
AR8151 POWER

AR8161 POWER

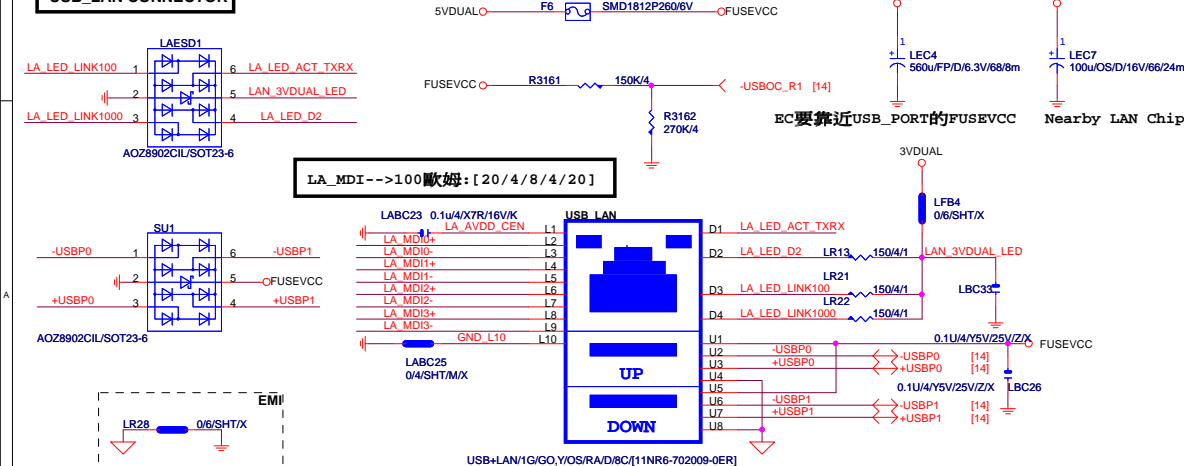
Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A



USB LAN CONNECTOR



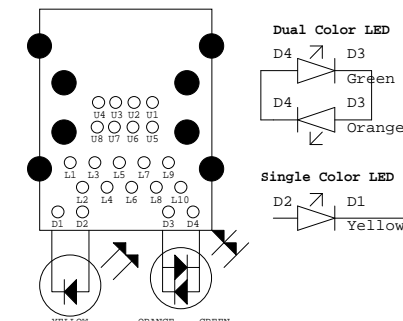
注意:LAN LED PROTECT:(CO-LAYOUT)
1.ESD(6PIN):AOZ8902CIL/SOT23-6(DEFAULT)
2.SURGE(5PIN):AZ2025-04S/SOT23-5L

注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]

料號	規格	廠商
11NR6-702009-0ER	1G LAN (12core)	UDE
11NR6-702009-91R	1G LAN(8 core)	FOXCONN
11NR6-702009-92R	1G LAN(8 core)	UDE
11NR6-702009-11R	1G LAN(12core/RED)	UDE
11NR6-702009-12R	1G LAN(8 core/RED)	FOXCONN

USB LAN BOM區分:

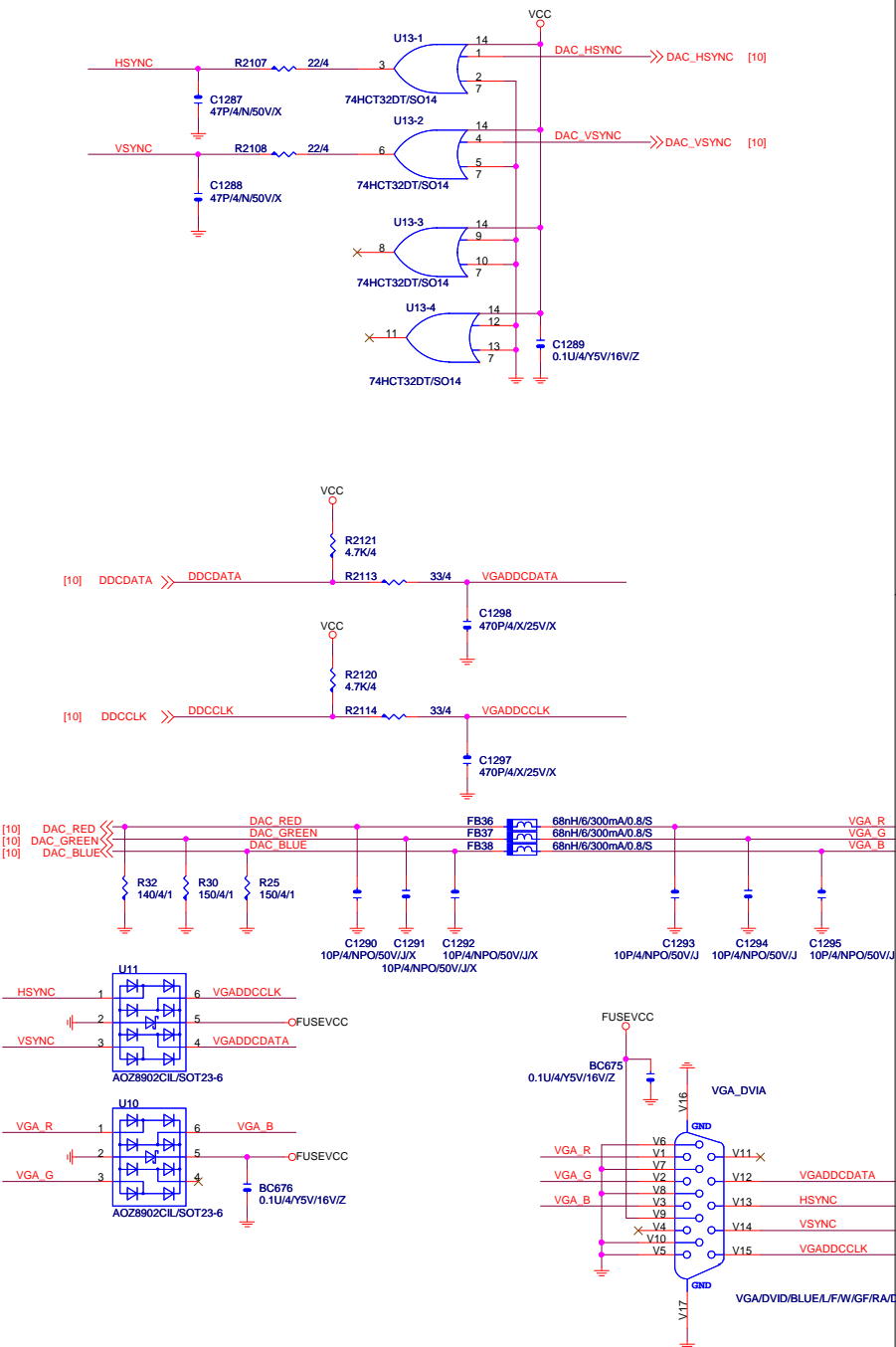
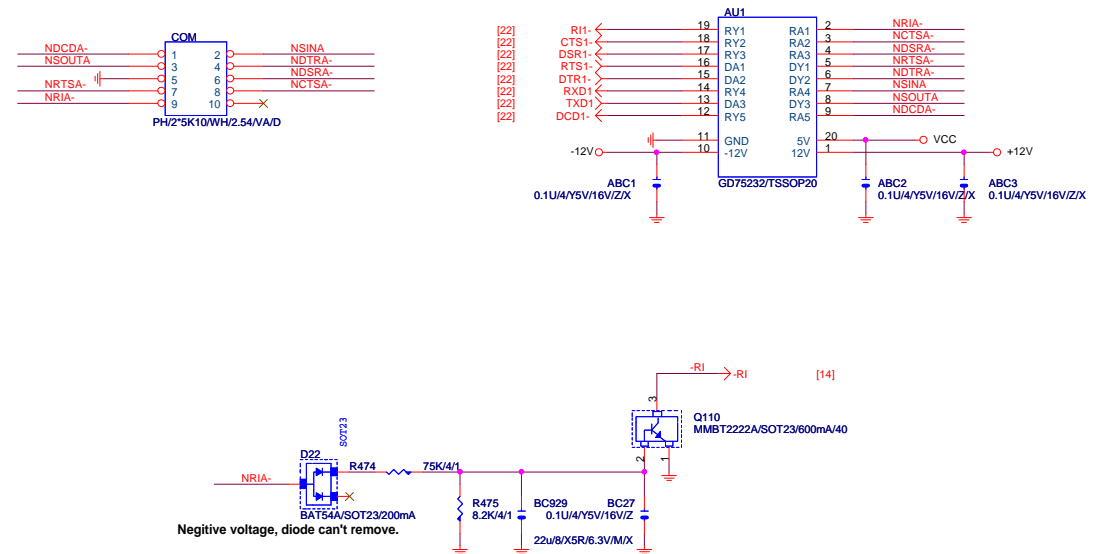
1. (紅色/12CORE/三倍):USB+LAN/1G/GO,Y/OS/RA/D/1/RED
2. (黑色/12CORE):USB+LAN/1G/GO,Y/OS/RA/D/1
3. (黑色/8CORE):USB+LAN/1G/GO,Y/OS/RA/D/8C



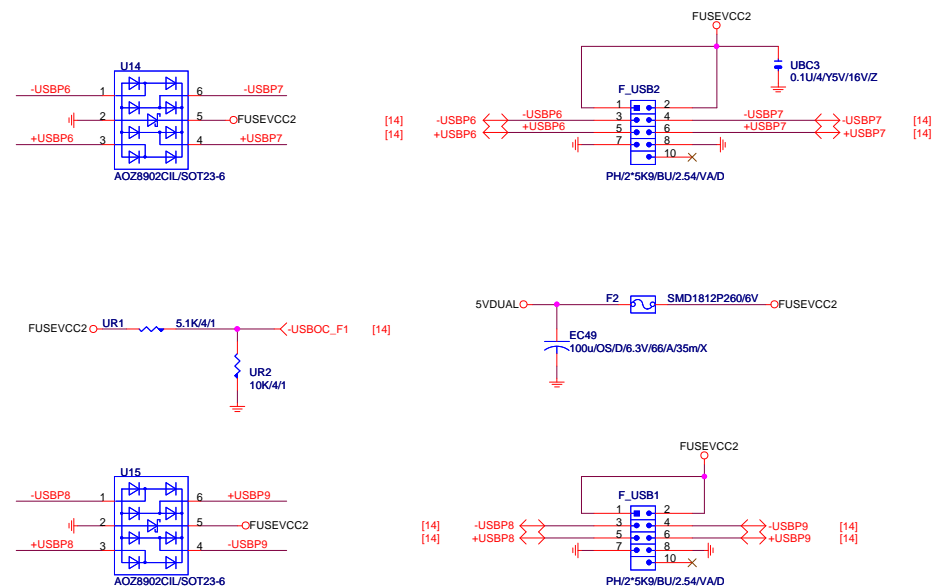
GIGABYTE

Title			
LAN AR8151			
Size	Document Number	Rev	
Custom	GA-880GM-D2H	4.0	
Date:	Friday, August 26, 2011	Sheet	19 of 29

D-SUB

**COM**

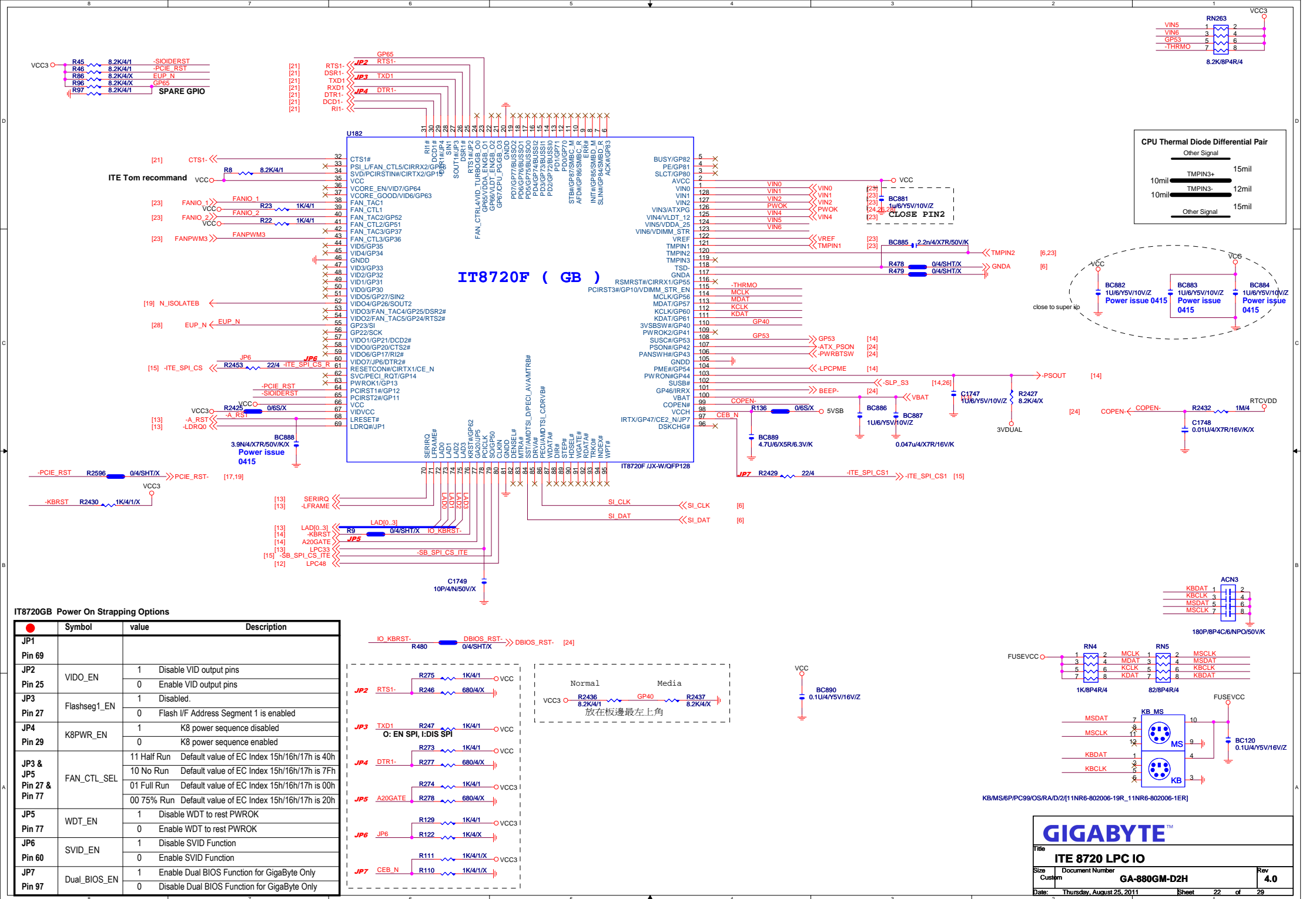
Front USB



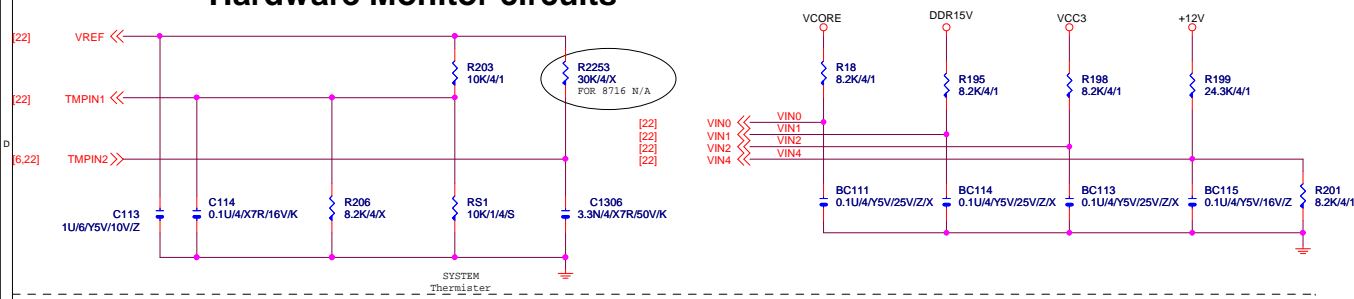
GIGABYTE

Title	RGB .TV CONNECTOR
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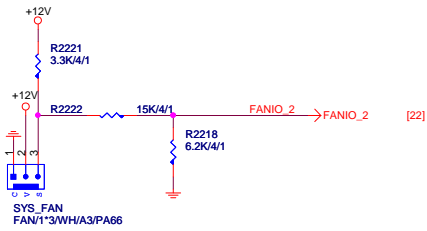
Size Custom	Document Number GA-880GM-D2H	Rev 4.0
Date: Thursday, August 25, 2011	Sheet 21 of 29	



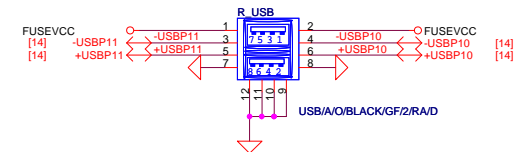
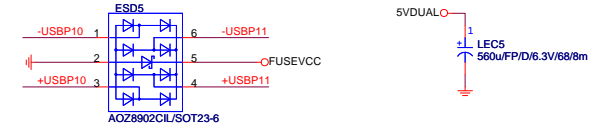
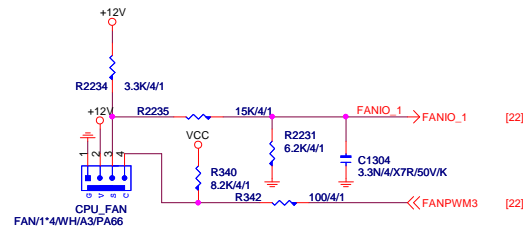
Hardware Monitor circuits

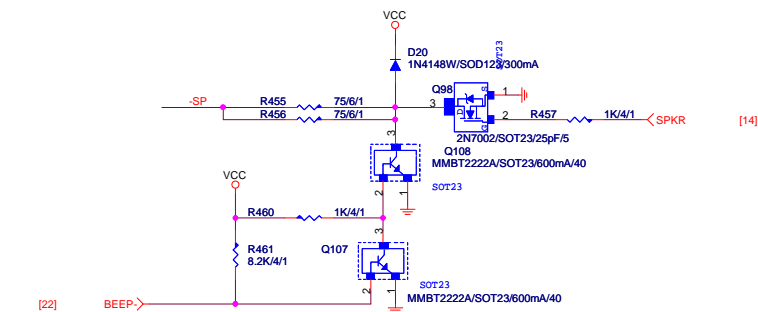
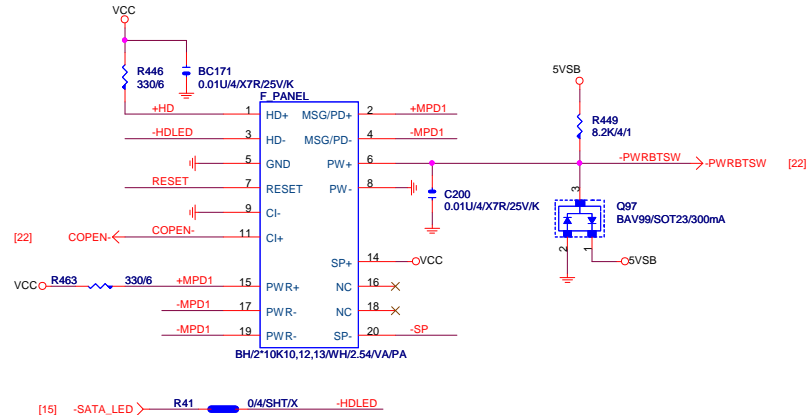


SYSTEM FAN

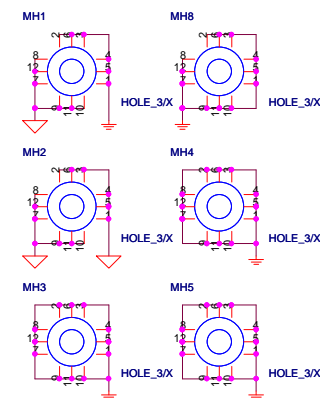
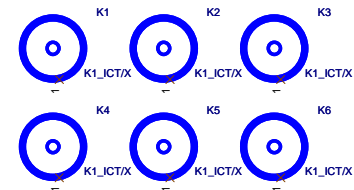
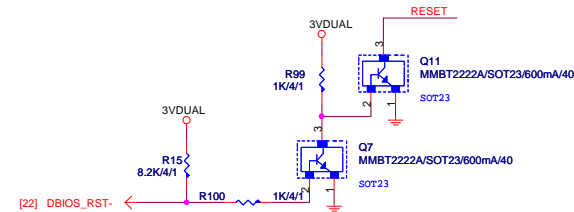
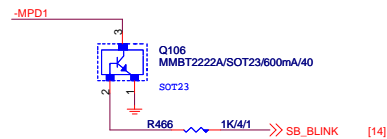
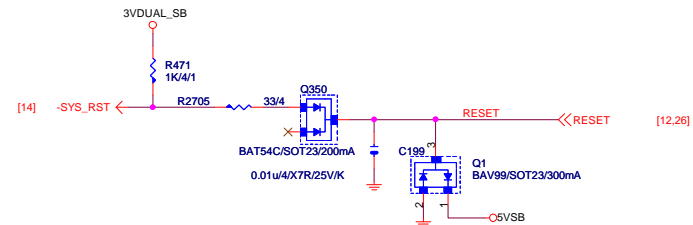
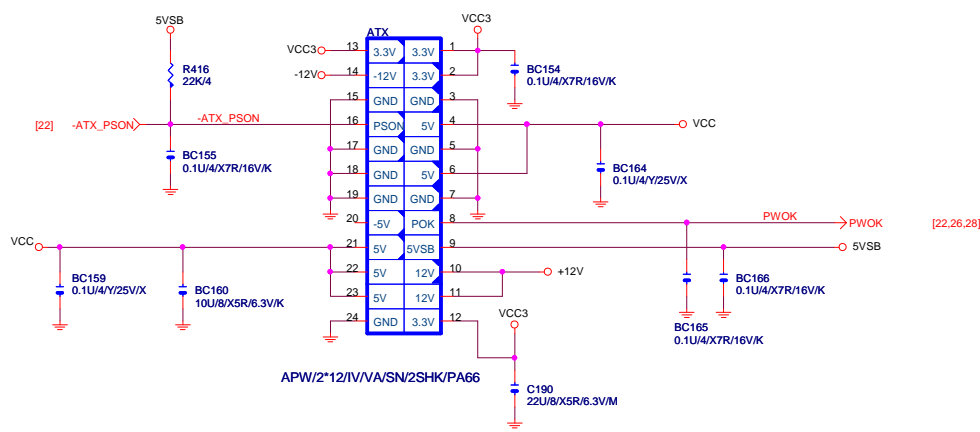


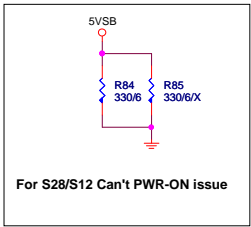
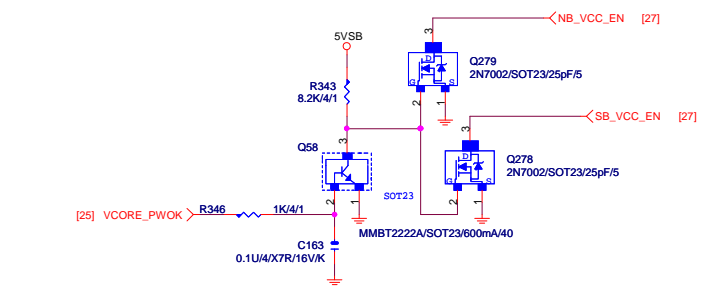
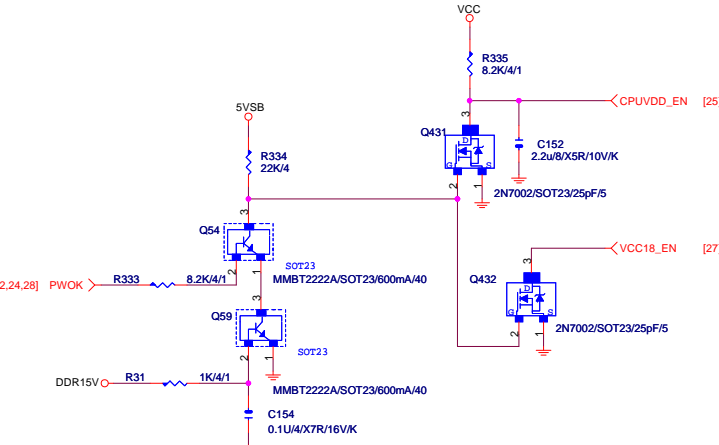
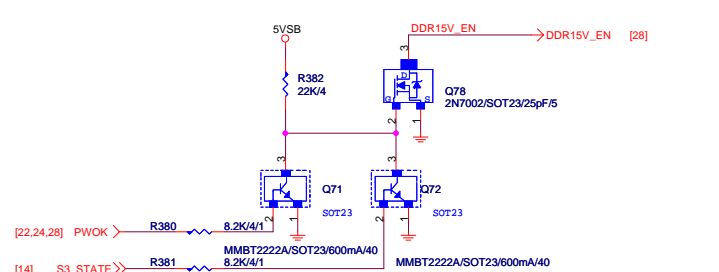
CPU FAN





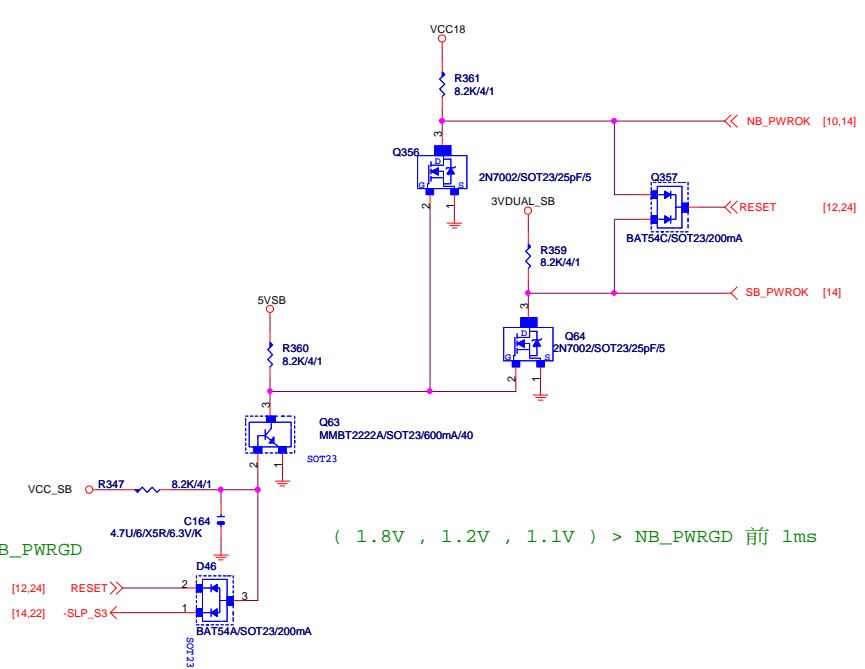
ATX POWER CONNECTOR

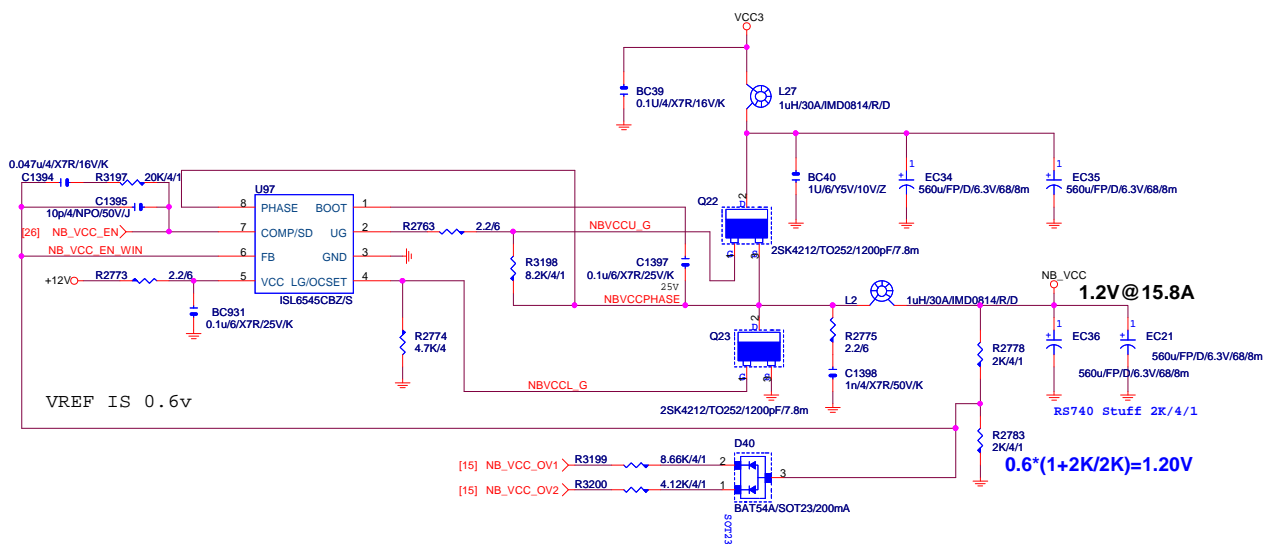




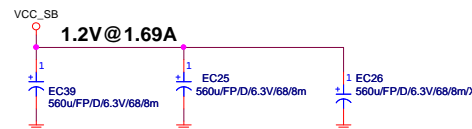
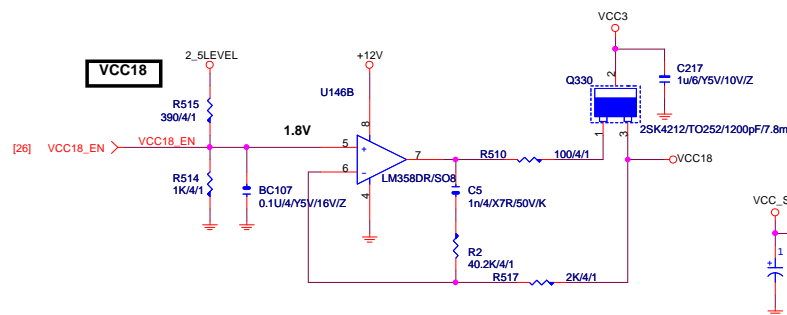
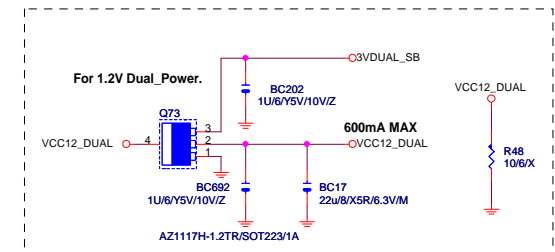
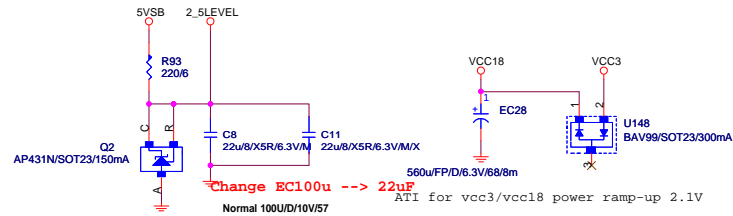
PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

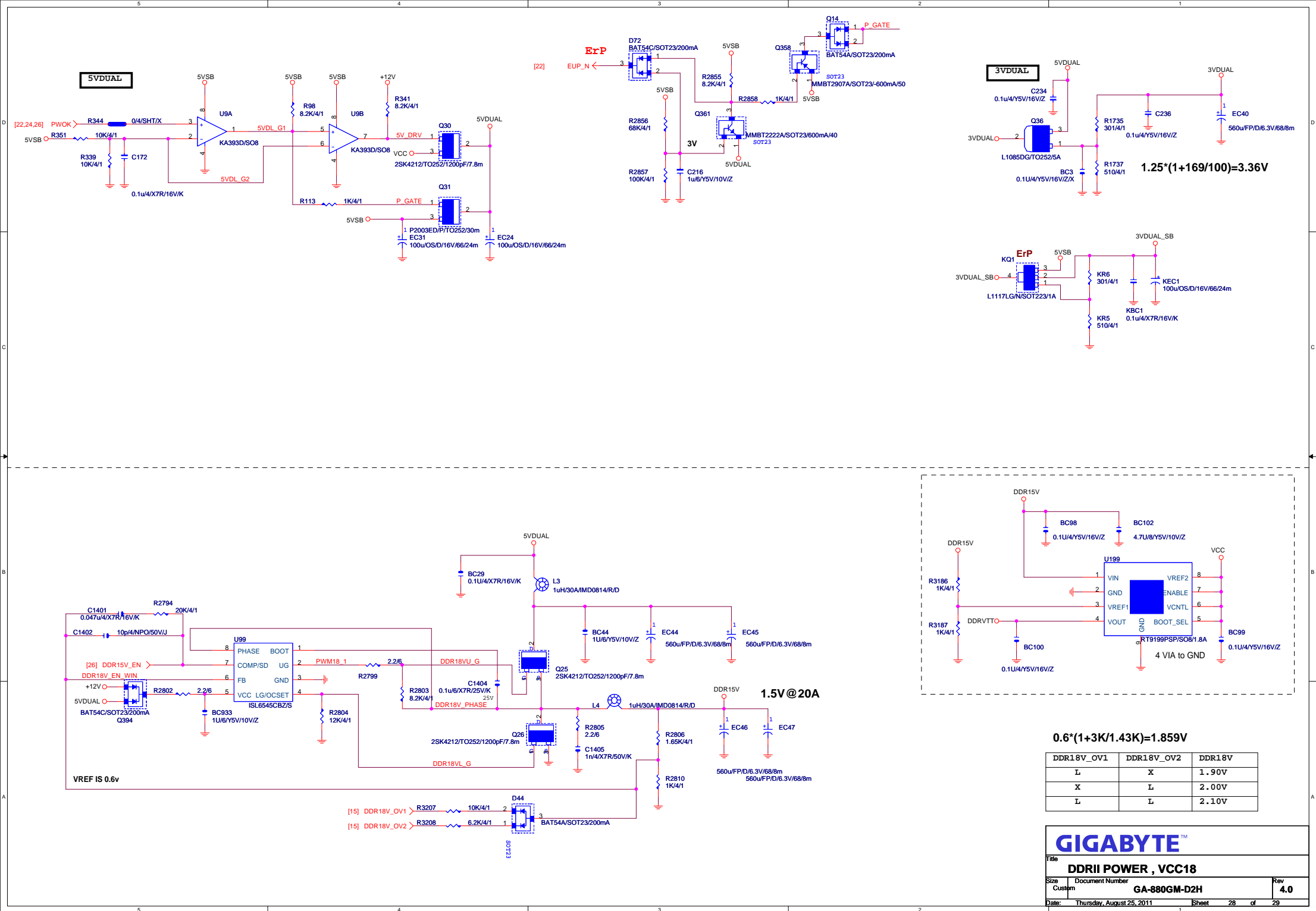




NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V



0.6*(1+3K/1.43K)=1.859V

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

GIGABYTE™

DDRII POWER , VCC18

Title	Document Number	Rev
Size	Custom	4.0
Date:	Thursday, August 25, 2011	Sheet 28 of 29

